

SPICE Device Model SUM110P06-08L

Vishay Siliconix

P-Channel 60-V (D-S) 175°C MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

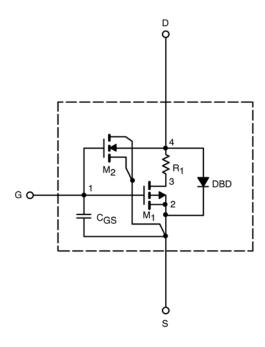
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to $125^{\circ}\mathrm{C}$ temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	2		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	702		А
Drain-Source On-State Resistance ^a		$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}$	0.0068	0.0065	Ω
		$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}, T_J = 125^{\circ}\text{C}$	0.0104		
	r _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}, T_J = 175^{\circ}\text{C}$	0.0123		
		$V_{GS} = -4.5 \text{ V}, I_D = -20 \text{ A}$	0.0083	0.0085	
Forward Voltage ^a	V_{SD}	I _F = -50 A, V _{GS} = 0 V	0.91	1	V
Dynamic ^b	•		•		
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$	8857	9200	pF
Output Capacitance	C _{oss}		975	975	
Reverse Transfer Capacitance	C _{rss}		760	760	
Total Gate Charge ^c	Q_g	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -110 \text{ A}$	175	160	nC
Gate-Source Charge c	Q_{gs}		40	40	
Gate-Drain Charge ^c	Q_{gd}		36	36	

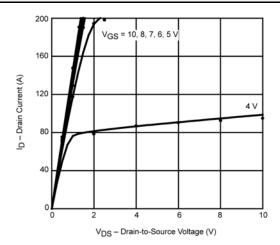
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.

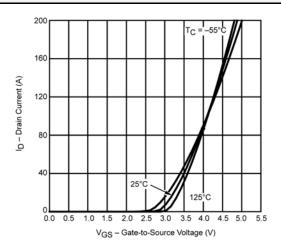


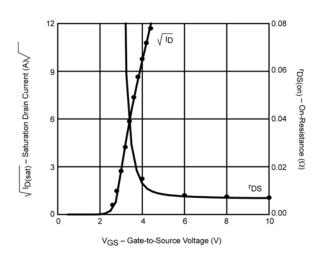
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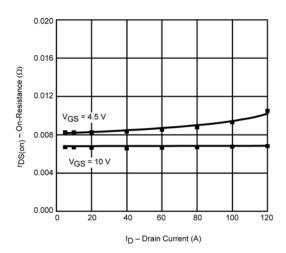
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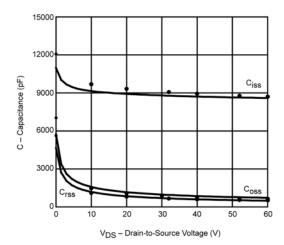
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

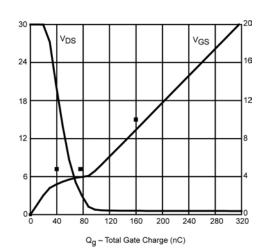












Note: Dots and squares represent measured data.



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